

REMARKS**Claim Rejections Under 35 U.S.C. § 103**

Claims 1-5, 7-11 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eitan* (U.S. Patent No. 6,552,387) in view of *Ling* (U.S. Patent No. 5,811,852). Applicant respectfully traverses this rejection.

Claims 1, 9, and 23 have been amended to make it clear that a separate oxide layer is formed above each source/drain region. Support for this amendment is found in the present specification at paragraph 0026 and Figure 2 of the present drawings. Therefore, no new matter has been added by this amendment.

Eitan discloses a non-volatile EEPROM comprising a non-conducting charge trapping dielectric. A single oxide layer 56 is formed over the substrate between the source 58 and drain 60.

Applicant's invention as claimed in the amended claims is to a planar NROM device that has an ultra-thin silicon-on-insulator layer with two source/drain regions separated by a normally fully depleted body. The claimed invention further includes a separate oxide layer over each source/drain region. This is neither taught nor suggested by *Eitan*.

Ling discloses a memory cell formed in a silicon-on-insulator wafer. There is no teaching or suggestion in *Ling* regarding a separate oxide layer formed over each source/drain region as currently claimed.

Even if it were obvious to combine *Eitan* with *Ling*, the combination still would not anticipate the present invention as claimed in the amended claims.

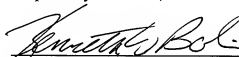
CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

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